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A Comparative Analysis on All Digital Phase Locked–Loops

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Abstract—*In this paper we have designed and implemented two all-digital phase – locked loop models one with an XOR gate as phase detector and the other with edge triggered JK flip flop as Phase Detector. The proposed models are implemented by using Very High Speed Integrated Circuit Hardware Description Language. The simulation has been performed in ISE Xilinx 14.2 software platform to study the power consumptions and synthesis characteristics of the models. The power consumptions of the models are evaluated from Xilinx Power Estimator. It is observed that the power consumption of the model with XOR gate and with edge triggered JK FF phase detector are recorded to be 15 mW and 21 mW respectively at ambient temperature of 25° C.*

Keywords*: ADPLL, EXOR, phase detector, VHDL.*

1. INTRODUCTION

The phase locked loop (PLL) is a self - control closed loop system for tracking signal phase. It has a wide range of applications including analog and digital communications, and other electronic fields. The first PLL was introduced in 1923 by Edward Appleton that introduced Automatic Synchronization of triode oscillators which were basic elements of radio communications [1, 2]. In 1940s, the PLL was widely used in synchronization of horizontal and vertical sweep oscillators in television receivers for transmission of synchronized pulses [3]. In 1960, the single chip PLL integrated circuit (IC) was developed and it was used in various electrical engineering fields as well as in radio communication. In 1970, the design and implementation of digital PLL's (DPLL's) started because of the popularity of large-scale integrations (LSI's) [4]. The first All digital phase locked loop (ADPLL) was started in 1980 [5]. The advantages of digital PLL's over analog PLL's are (i) less sensitivity to dc drifts and component aging, (ii) ease in building higher order loops, (iii) no need for adjustment, (iv) ability to perform sophisticated signal processing on the IC chips, (v) more flexible and versatile. The classical DPLL's are still semi – analog circuit, therefore the ADPLL and the software controlled PLL (SCPLL) has gained increased attention [4]. The ADPLL's is implemented only by using digital blocks. ADPLL's have become lucrative due to its scalability, faster lock in time and easy redesign with process changes [6, 14].

In this work we have designed two ADPLL models with EXOR gate as PD and with edge triggered JK FF as PD and compare their results after simulation by using Very High Speed Integrated Circuit Hardware Description Language (VHDL).

2. REVIEW OF RELATED WORKS

In 1999, Nam Guk Kim et al. have proposed ADPLL to provide both large locking frequency range and good tracking performance. They observed that the model does not suffer from phase jitter due to the quantization effect of the numerically controlled oscillator [7].

In 2003, R. Stefo, J. Schreiter, J. U. Schlussler and R. Schuffny have designed a high resolution ADPLL frequency synthesizer model for FPGA- and ASIC-based applications. They implemented their model in 4OOBG432VIRTEX FPGA. They described the whole model using synthesizable VHDL [8].

In 2003, T. Olsson and P. Nilsson designed and fabricated a prototype all-digital PLL clock multiplier using a *0. 3 5* ~ CMOS process [9].

In 2006 C. H. Shan, Z. Chen and Wang, Y proposed an ADPLL model with double edge triggered D-FF. The model designed using VHDL and implemented on a prototype based on a chip of VIRTEX FPGA VCU400Bg432 [10].

In 2009 C. H. Shan, Z. Chen and J. Jiang designed an ADPLL system with high performance on wideband frequency tracking and also proposed a balance mechanism for improving system performance on noise. The system is designed by using VHDL and implemented on a FPGA chip [11].

In 2012 M. H. Shabaany and M. Saneei presented ADPLL with a new phase frequency detector and controlled oscillator with body-biasing for 0.1 – 1.1 GHz frequency range [12].

In 2014, A. Patil and R. Saini proposed a method of implementing a linear ADPLL based on FPGA to obtain high frequency resolution & short locking time. They designed the

ADPLL model using ISE Xilinx 9.2. They observed the centre frequency of the model is 100 kHz [13].

In 2016 N. Tripathi and S. N. Pradhan presented a power efficient design of ADPLL using digital loop filter instead of the conventional one. They implemented their model using Verilog HDL and is synthesized using Cadence RTL complier [6].

3. THE OBJECTIVE AND METHODOLOGY

The main objective of the proposed work is to design and implementation of ADPLL models with EXOR gate as PD and with edge triggered JK FF as PD. The simulation of the model has been performed in Xilinx 14.2 platform by using VHDL to study power consumption and synthesis details of the designed ADPLL model.

The methodologies towards implementation of the proposed work are: (i) each block of the model is design and simulated by using Xilinx 14.2., (ii) behavioral simulation of the overall model by integrating individual blocks is done to study various aspects of the model and (iii) XPE power estimator is used to calculate power consumption of the model.

4. PROPOSED ADPLL MODEL

In ADPLL, all components used are digital in nature. ADPLL consists of digital phase detector (PD), digital loop filter (LF) and digital controlled oscillator (DCO) which are connected to form a closed – loop feedback path as shown in **Fig.1.** The advancements of very - large scale integration circuits (VLSI's), APLL's have abilities to achieve the requirements of communication applications. The ADPLL is most widely used since FPGA is an exclusively a digital device where ADPLL is to be implement. The proposed ADPLL models with EXOR gate as PD and edge triggered JK FF as PD is shown in **Fig.2 (a) and (b) [6, 16, 17]**. Here K counter is used as digital LF and DCO is formed by combination of increment decrement counter (ID counter) and divide by N counter.

5. THE ANALYSIS OF INDIVIDUAL BLOCKS

Details of each individual blocks of the corresponding circuit of ADPLL model depicted in **Fig.2 (a) and (b)** are given below:

A. Digital PD

In this ADPLL design we have implemented two types of PD namely EXOR gate PD and edge triggered JK FF PD. It compares the phase of the input reference signal with the phase of the produced ADPLL output signal. It generates an error signal which is proportional to the phase difference between these two signals.

(i) EXOR PD

EXOR gate PD simply a two input EXOR gate that utilizes the property of EXOR gate. Since the EXOR gate produces output with logic high only when both the inputs are not equal and that can be seen as the phase difference between two inputs [15].

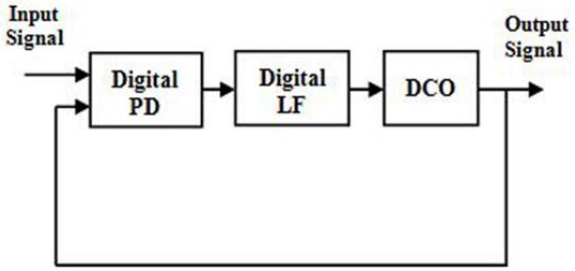

Fig. 1: Block diagram of ADPLL

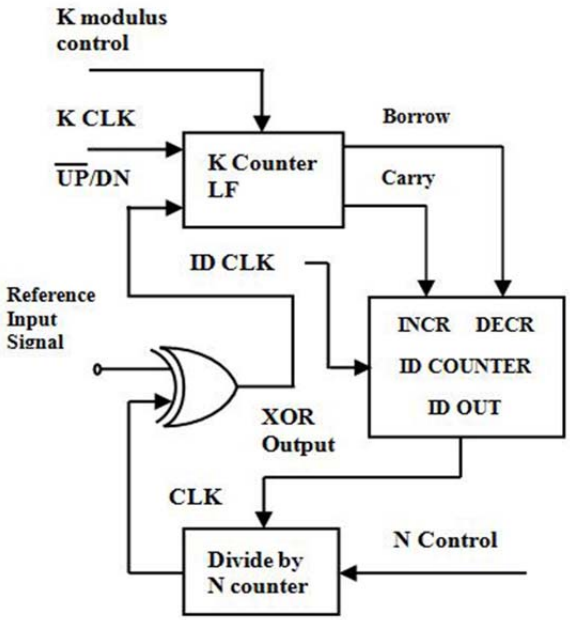

Fig. 2 (a). ADPLL circuit diagram with EXOR PD

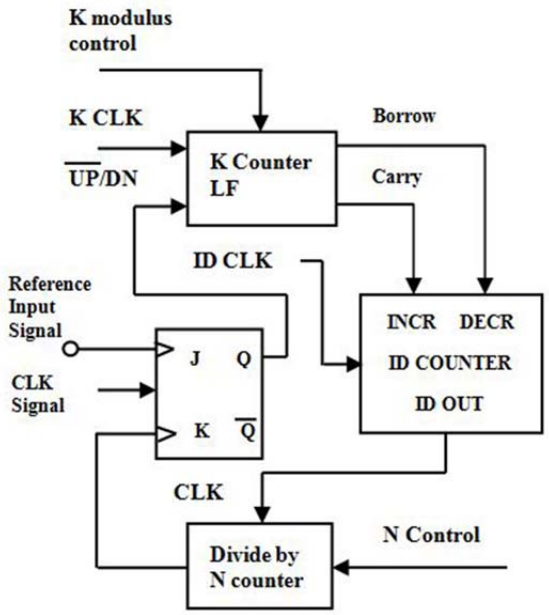

Fig.2 (b). ADPLL circuit diagram with JKFF PD

(ii) Edge triggered JK FF PD

It contains a JK FF with a clock input. JK FF is used as PD because it is a sequentially based circuit.

B. Digital LF

K counter is used as digital LF in this ADPLL design. K counter LF consists of two independent counters namely up counter and down counter that counts always upward. The content of both counters ranges from 0 to (K-1) where K is controlled by K modulus control input and always power of two [6]. When UP/DN signal is high, the down counter is active and the contents of the up counter stay frozen. Similarly, when UP/DN signal is low, the up counter is active and the contents of the down counter stay frozen. The up and down counter produces carry and borrow output respectively which are the MSB bits of the both counter. Both counter reset to zero when the counter contents exceeds the maximum count (K-1) [5, 6].

C. DCO

ID counter and divide by N counter is used as DCO in this implementation. The ID counter consists of three inputs: a clock input, increment and decrement. The carry of the K counter LF is assigned to increment (INCR) input and borrow is assigned to decrement (DECR) input. When carry pulse appears at the INCR input then the next ID output pulse is advanced in time by one ID clock period and when borrow pulse appears at the DECR input then the next ID output pulse is delayed in time by one ID clock period [5]. ID counter output is fed to the divide by N counter.

6. THE SIMULATIONS

Simulation of the proposed model is done by using VHDL code in Xilinx 14.2 software. The schematic diagram of synthesized ADPLL models with EXOR gate as PD and with JK FF as PD are shown in **Fig.3 (a) and (b)** respectively. The behavioural simulation results for both cases are shown in **Fig. 4 (a) and (b)**. From the simulation results it is observed that ADPLL model with EXOR gate as PD, locked after ten clock cycles and ADPLL with edge triggered JK FF as PD model locked after six clock cycles.

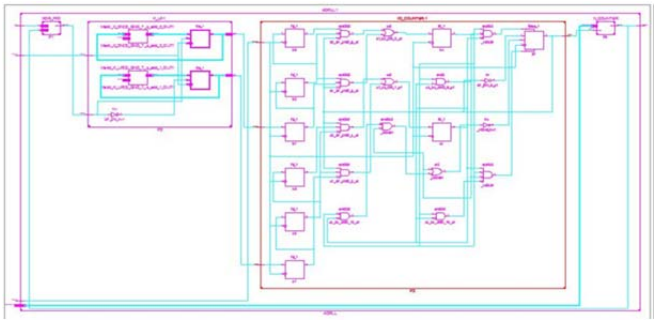

Fig. 3 (a). Schematic representation of ADPLL with EXOR gate as PD

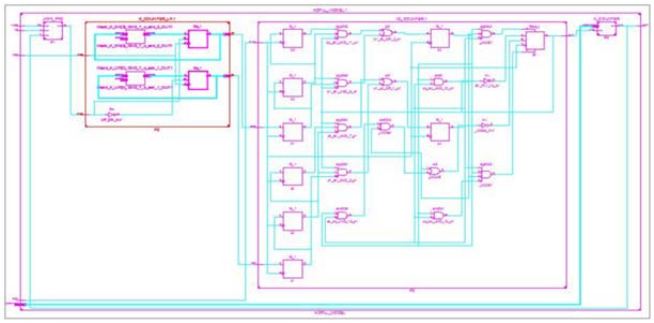

Fig. 3 (b). Schematic representation of ADPLL with JK FF as PD model

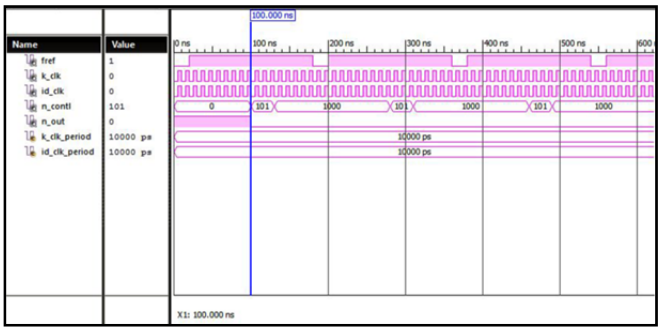

Fig. 4 (a). Simulation result for ADPLL with EXOR gate as PD model

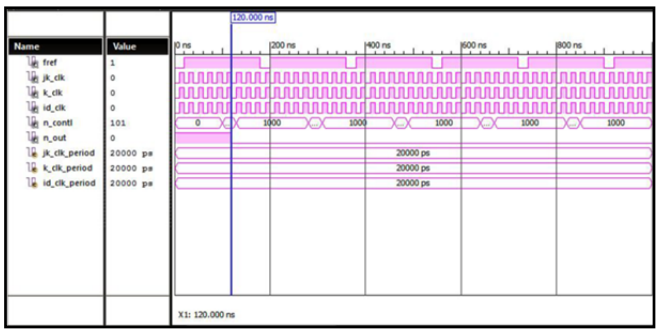

Fig. 4 (b). Simulation result for ADPLL with JK FF as PD model

7. RESULTS AND DISCUSSION

The result obtained from the synthesis are given in **Table 1 and Table 2** for ADPLL model with EXOR gate as PD and model with edge triggered JK FF as PD. A comparison with obtained result and the previous work is given in **Table 3.** From the simulation results it is observed that JK FF ADPLL model has faster locking time than the EXOR PD model. The total power consumption for ADPLL with EXOR gate PD model is 15 mW. Dynamic as well as quiescent power consumption is recorded as 1 mw and 14 mW for EXOR gate PD model. The total power consumption for JK FF as PD model is 21 mW as Dynamic and quiescent power consumption are recorded 1 mw and 20 mW respectively.

Table 1: Power consumption of ADPLL models

SL NO.	Model /Parameters	Total Power consumption (mW)	Temp. (° C)	Device Family
1	EXOR gate PD	15	25	Spartan6
2	Edge triggered JK FF PD	21	25	Spartan6

Table 2: Synthesis details of ADPLL models

SL NO.	Logic Utilization	ADPLL Model with EXOR as PD			ADPLL Model with edge triggered JK FF as PD		
		Used	Available	Logic Utilization	Used	Available	Logic Utilization
1	Number of Slice used as Flip flops	22	4,800	1%	23	18,244	1%
2	Number of Slice LUTs	17	2,400	1%	18	9,112	1%
3	Number of occupied Slices	8	600	1%	9	2,278	1%
4	Number of bonded IOBs	4	102	3%	5	232	2%

Table 3. Comparison of the ADPLL models with the previous work

SL NO.	Parameters	Proposed model with EXOR PD	Proposed model with JK FF PD	Previous work	Traditional ADPLL
1	Power consumption (Watt)	0.015	0.021	0.485 [Ref 16]	0.561
2	IO Utilization (bonded IOB)	4/102	5/232	6/600 [Ref 16]	4/480
3	Number of Slice LUTs	17/2,400	18/9112	135/297600 [Ref 16]	26/28800
4	Number of Slice flip flops	22/4,800	23/18224	45/9,312 [Ref 17]	-
5	Number of occupied Slices	8/600	9/2,278	71/4,656 [Ref 17]	-

8. CONCLUSION

From the present study model it can be concluded that the locking speed of edge triggered JK FF ADPLL model is faster than the ADPLL model with EXOR gate as PD. As such, edge triggered JK FF ADPLL can be used for high speed communication with the expense of higher power consumption than ADPLL with EXOR gate as PD.

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